Model Name:MRNM7AP

Revision 1.0

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	PWRGD&RESET MAP
05	POWER DELIVERY CHART
06	CPU_1-PCIE_DMI_FDI_eDP
07	CPU_2-MEM Controller
08	DDRIII CHANNEL A,B
09	CPU_3-PWR
10	CPU_4-GND
11	HDMI,mDP
12	NM70_FDI, DMI,USB,PCI
13	NM70_DISPLAY,GPIO
14	NM70_HOST,SATA,HDA,SPI
15	NM70_CLK BUFFER,PCIE
16	NM70_PWR
17	NM70_GND
18	SIO ITE8773 , FAN,FP
19	AUDIO CODEC ALC887
20	AUDIO JACK
21	RTL8111E-CG/RTL8105E-H
22	LINNER POWER-1
23	DISCRETE POWER
24	AD19V & VCC5 & VCC3
25	VCORE & VCPU_VAXG NCP6131
26	
27	

SHEET	TITLE
28	
29	
30	
31	
32	
33	

GIGABYTE TECHNOLOGIES , INC.

Title	Cover Sheet	
Size: Custom	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 1 of 25	

Model Name: MRHM7AP-LF

Revision 0.1

Component value change history

2012/07/31

Data	Change Item	Reason

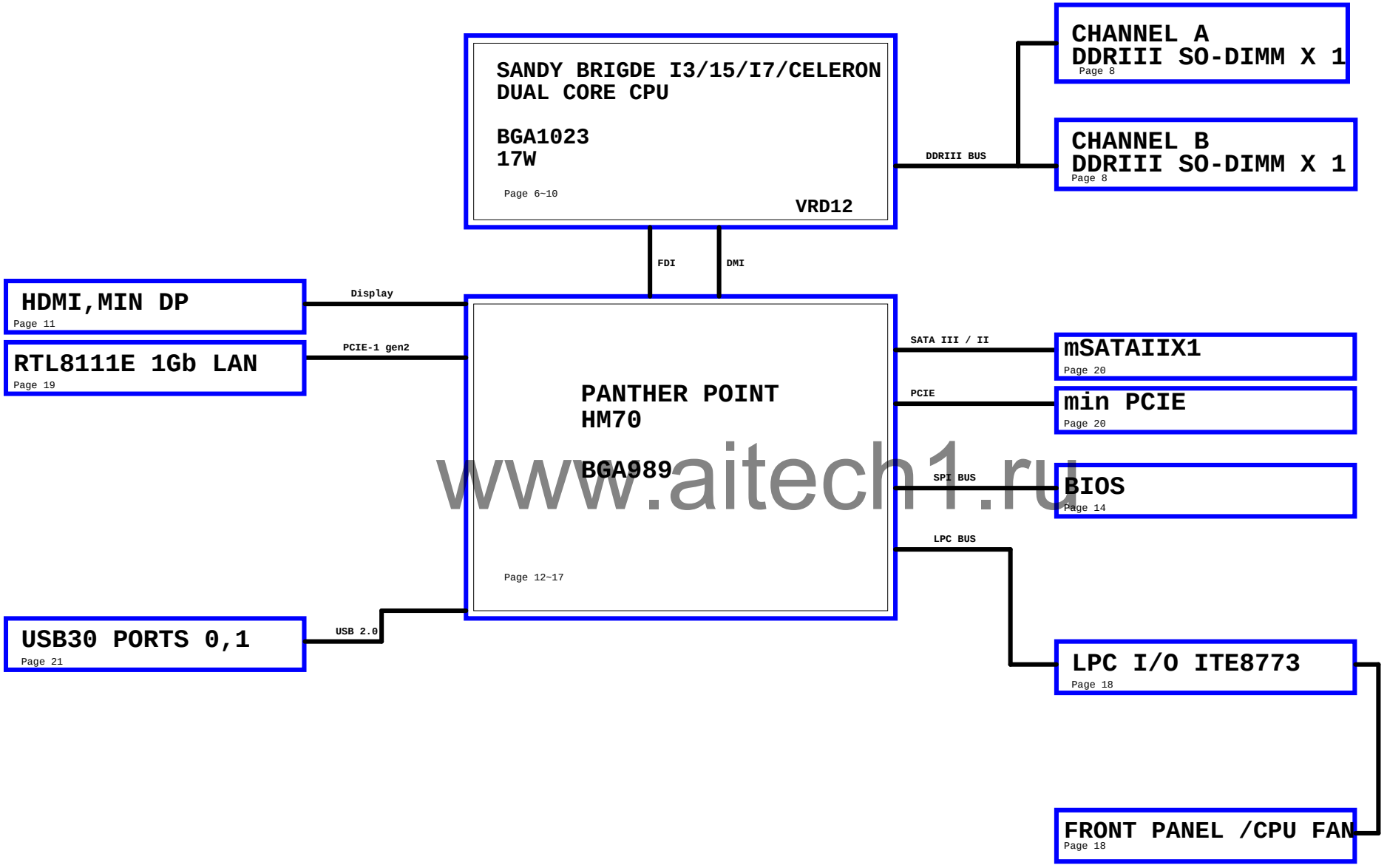
Circuit or PCB layout change

DATE	Change Item	Reason

GIGABYTE TECHNOLOGIES , INC.

Title	BOM & PCB MODIFY HISTORY	
Size: Custom	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 2 of 25	

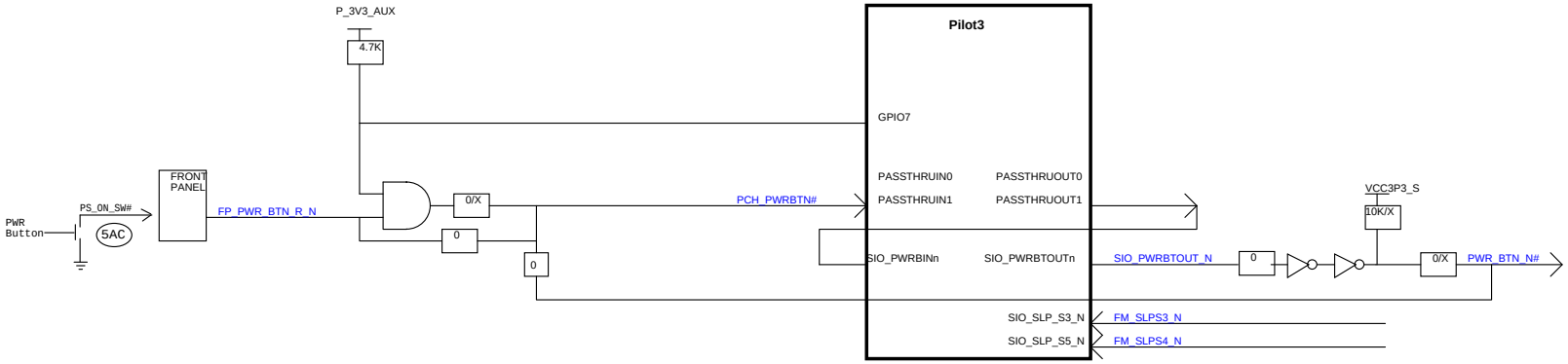
BLOCK DIAGRAM

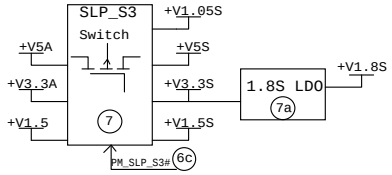


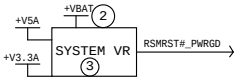
GIGABYTE TECHNOLOGIES , INC.

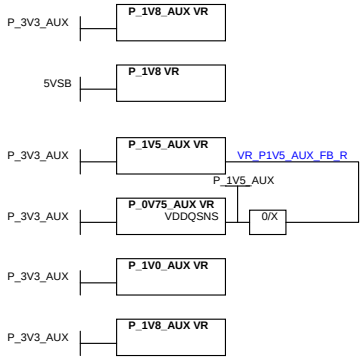
Title: BLOCK DIAGRAM		
Size: C	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 3 of 25	

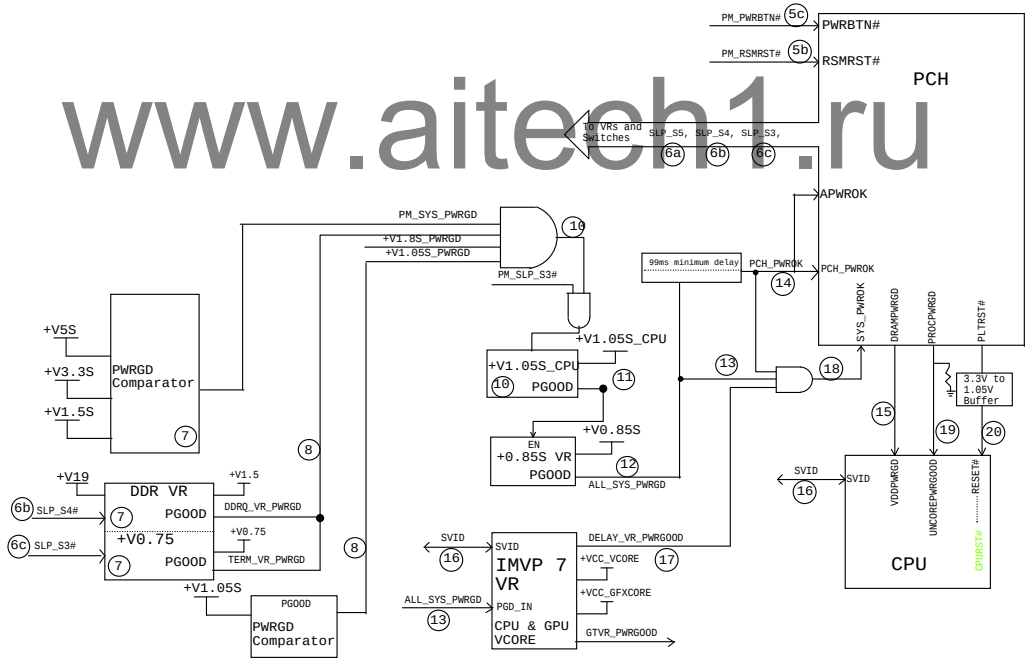
Huron River Power Up Sequence Diagram



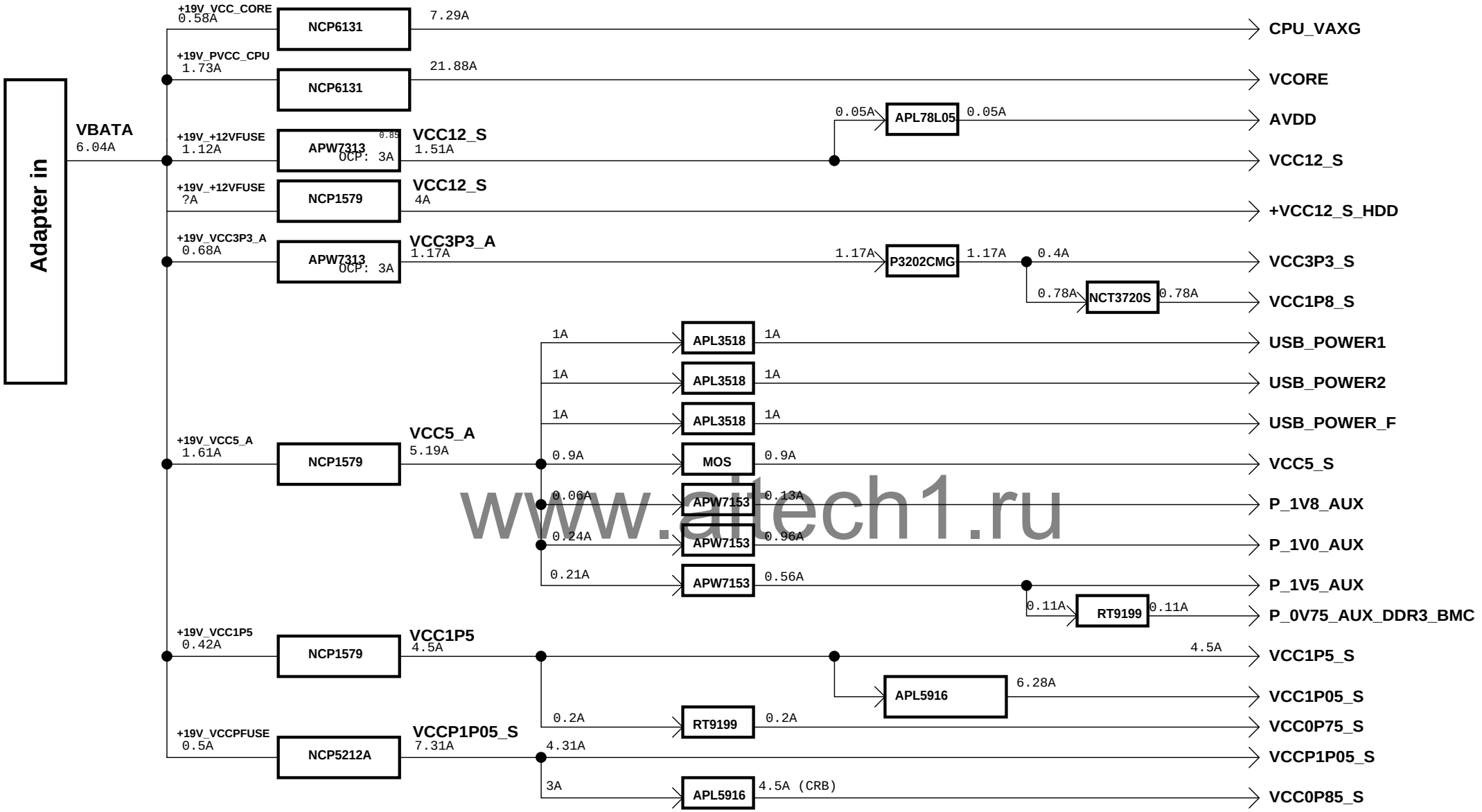








Title	PWRGD&RESET MAP	
Size: Custom	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 4 of 25	



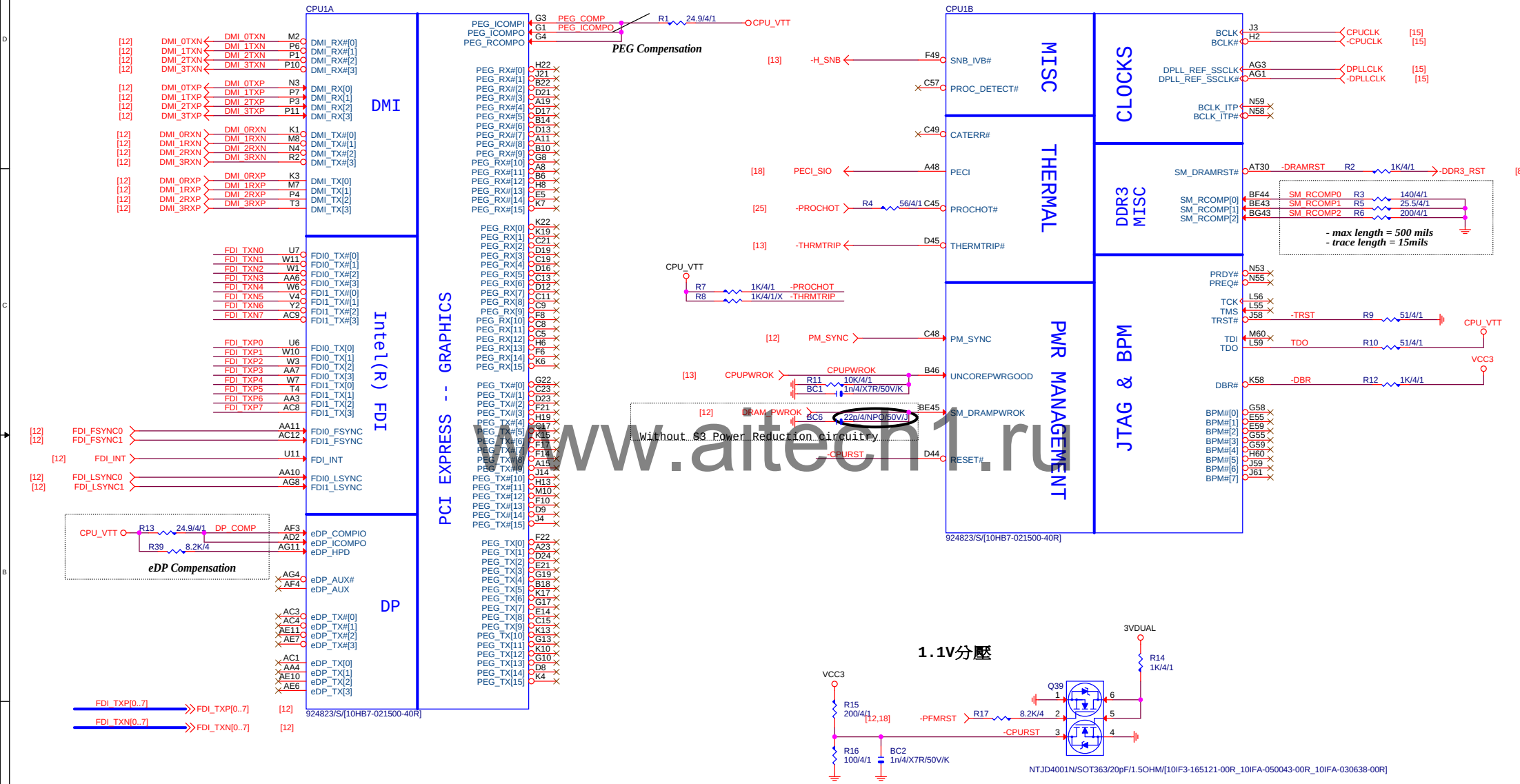
Title	POWER DELIVERY CHART	
Size B	Document Number MRNM7AP	Rev 1.0
Date: Thursday, May 02, 2013	Sheet 5 of 25	

Sandy Bridge 2C BGA Processor (DMI,DP,PEG,FDI)

Sandy Bridge 2C BGA Processor (CLK,MISC,JTAG)

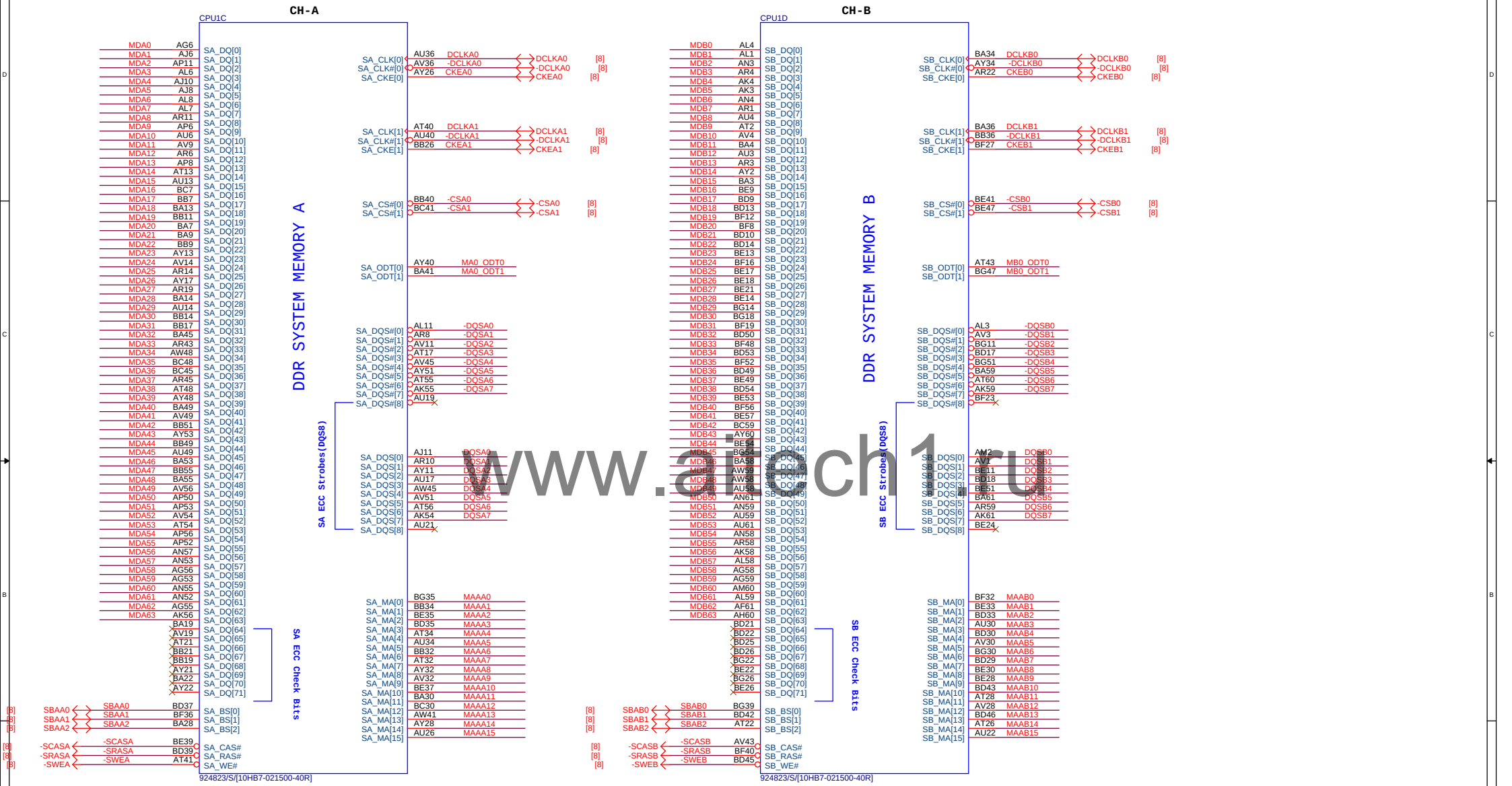
Please don't reversal DMI and FDI lane.

PEG_ICOMPO 12 mils



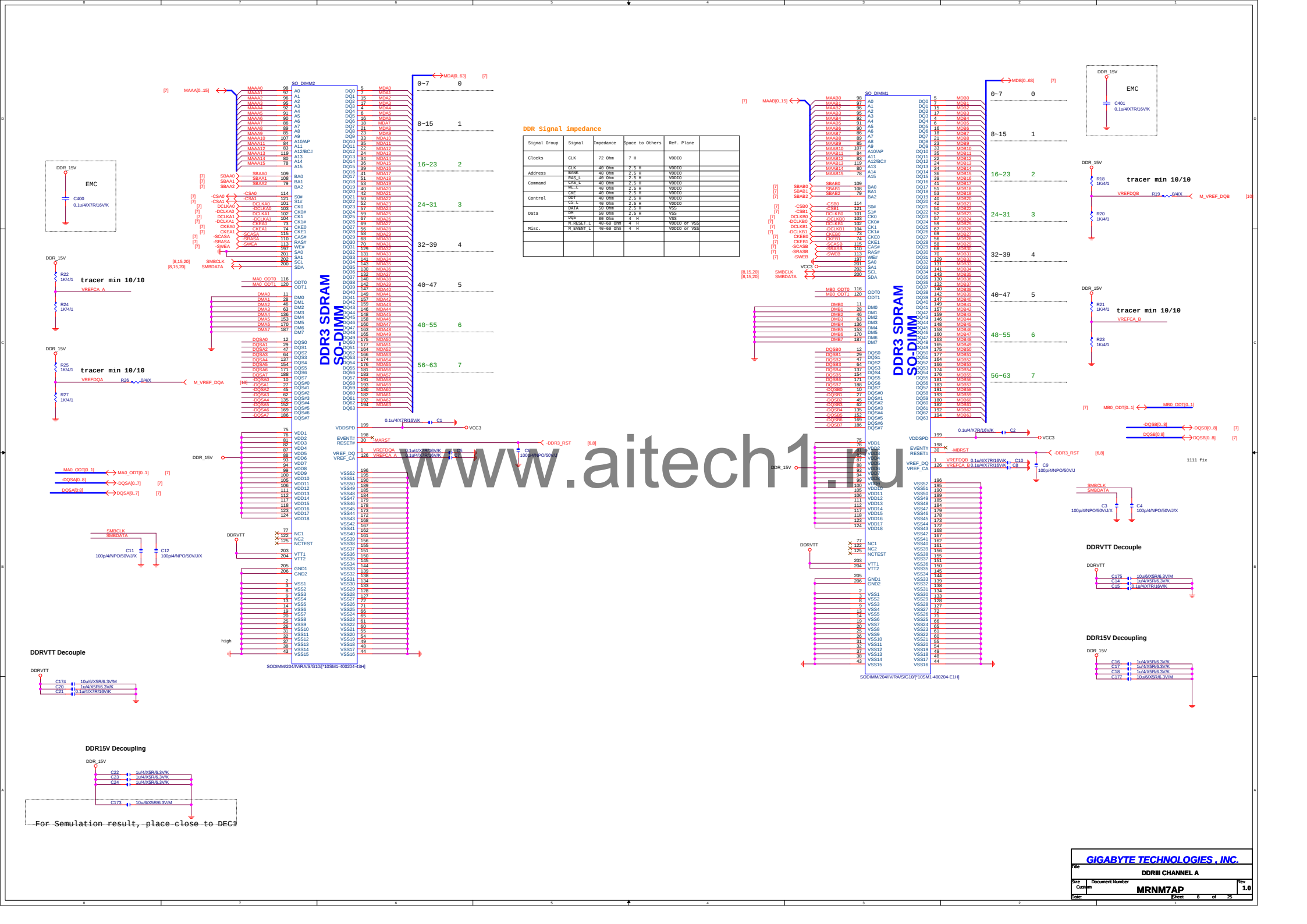
GIGABYTE TECHNOLOGIES , INC.			
Title	Sandy Bridge--DMI, FDI, eDP, PEG		
Size	Document Number MRNM7AP		Rev 1.0
Date: Thursday, May 02, 2013	Sheet 6 of 25		

Sandy Bridge 2C BGA Processor (DDR3)

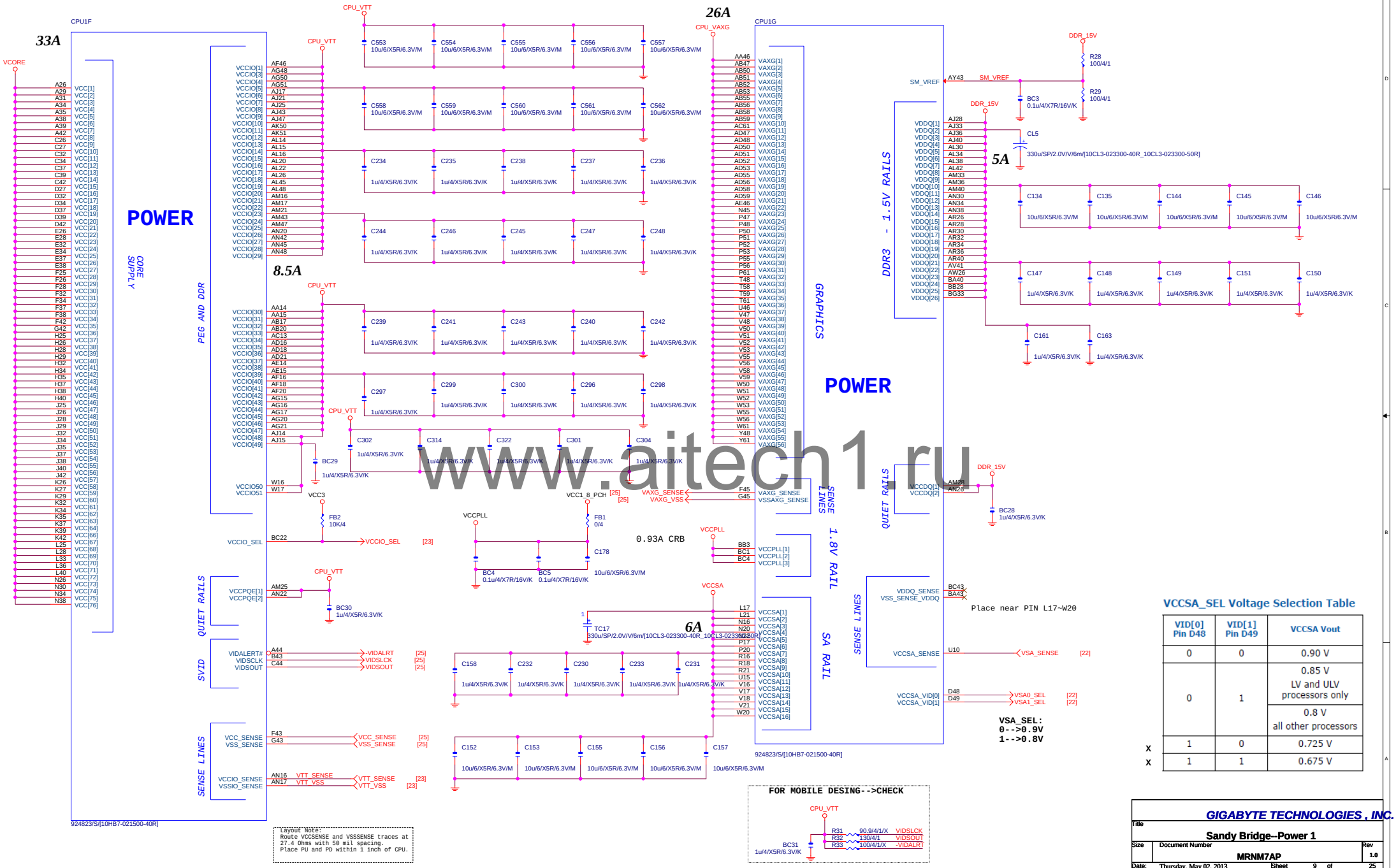


Title	Sandy Bridge--Memory
Size	Document Number: MRNM7AP
Rev	1.0
Date:	Thursday, May 02, 2013
Sheet	7 of 25

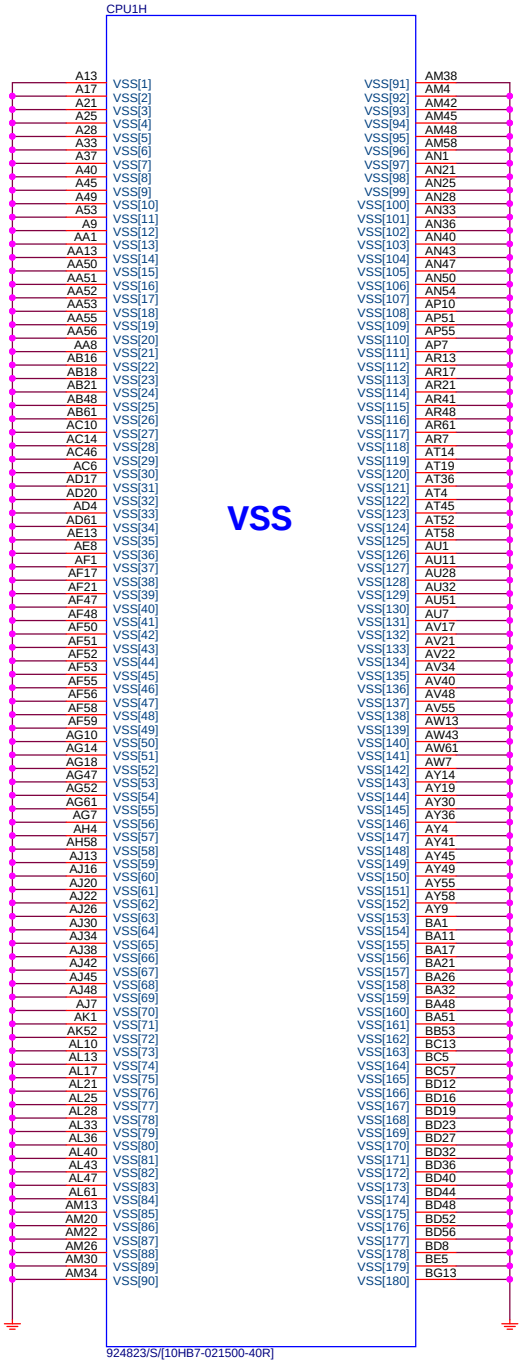
GIGABYTE TECHNOLOGIES , INC.

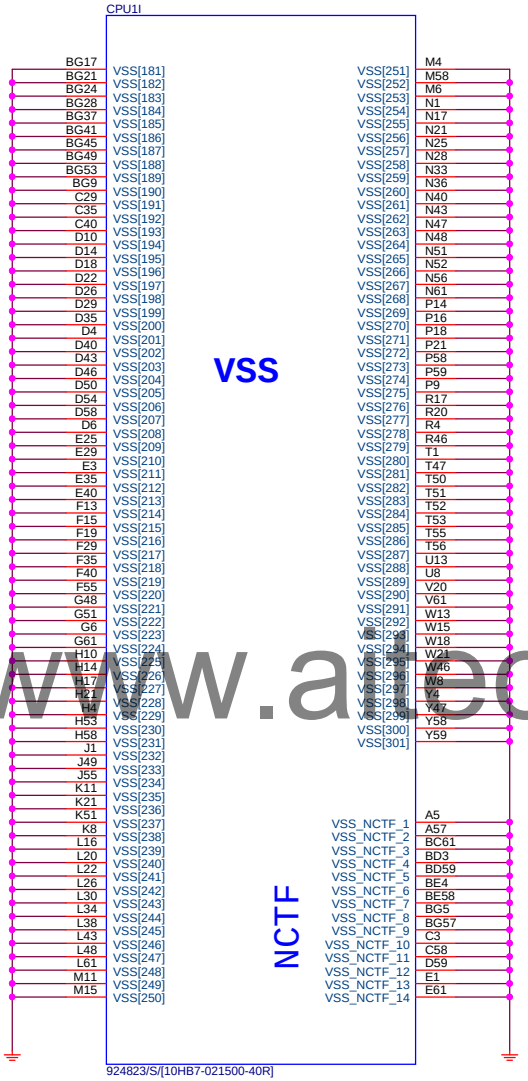


Sandy Bridge 2C BGA Processor (Power)

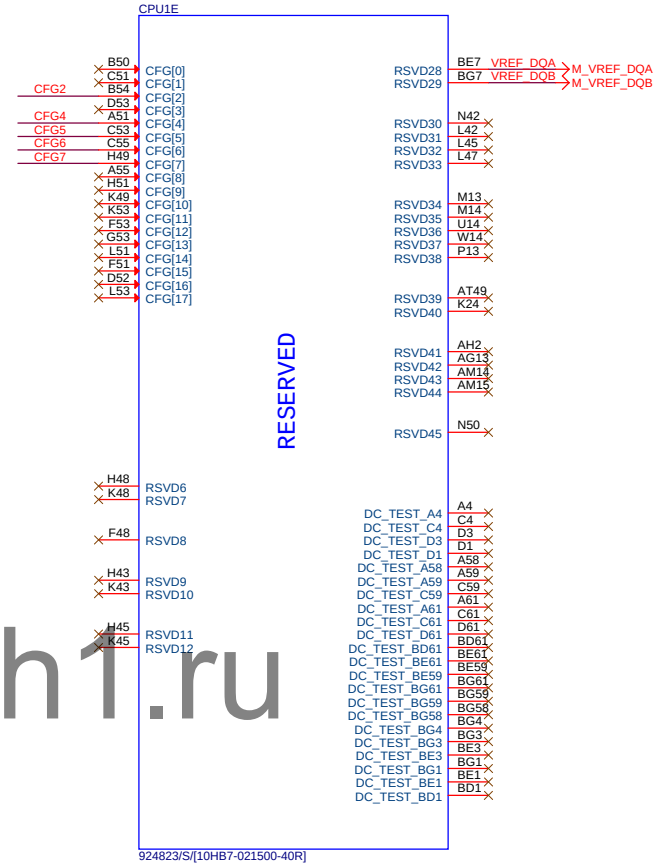


Sandy Bridge 2C BGA Processor (GND)





Sandy Bridge 2C BGA Processor (Reserved)



CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	**NORM**	**Reverse**	LANE REVERSAL[0],x16
3	RSVD	RSVD	RSVD
4	**DISABLE**	**ENABLE**	eDP ENABLE
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIE CONFIG
1	1	1X16 , Default
1	0	2X8
0	1	RSVD
0	0	X8,X4,X4

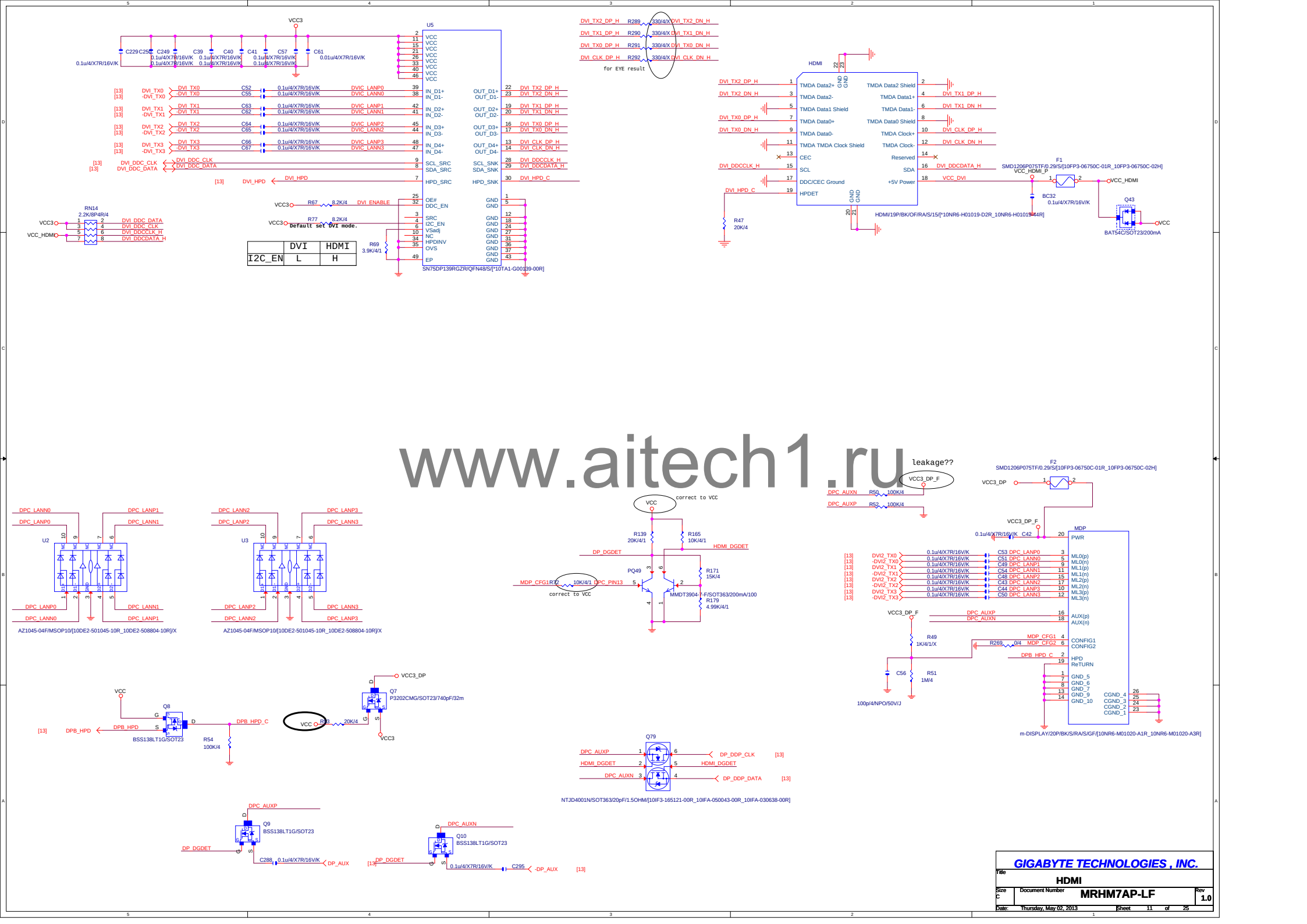
CFG 0-17 all internal PULL-UP

CFG2 R34 1K/4/1/X

CFG4 R35 1K/4/1/X
CFG5 R36 1K/4/1/X
CFG6 R37 1K/4/1/X
CFG7 R38 1K/4/1/X

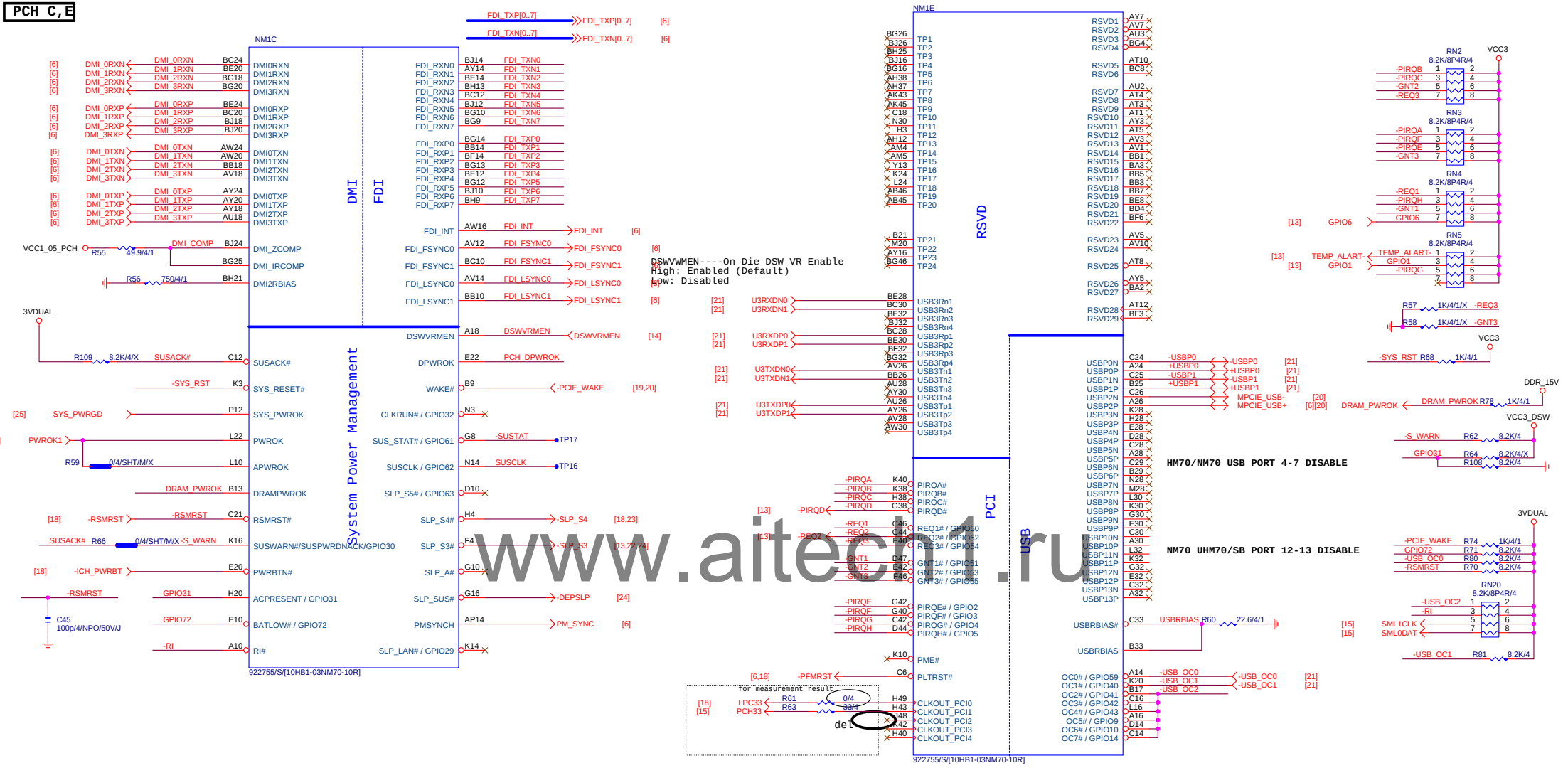
GIGABYTE TECHNOLOGIES , INC.

Title	Sandy Bridge --GND	
Size	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 10 of 25	



Company	GIGABYTE TECHNOLOGIES , INC.
Title	HDMI
Size	C
Document Number	MRHM7AP-LF
Rev	1.0
Date	Thursday, May 02, 2013
Sheet	11 of 25

PCH C,E



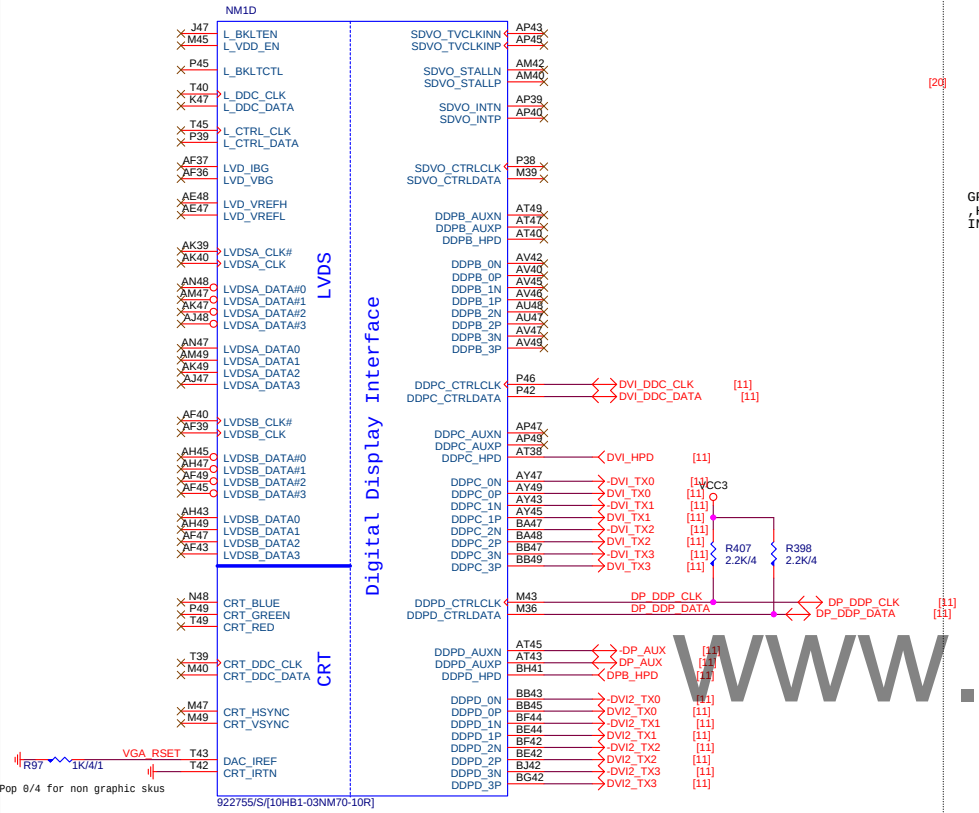
FOR FUSE SHORT GPIO

USB OC# Configure	
OC0#	USB0,1(USB2_1)
OC1#	USB2,3(USB2_2)
OC2#	USB4,5(NM70:N/A)
OC3#	USB6,7(NM70:N/A)
OC4#	USB8,9(F_USB2_1)
OC5#	USB10~11(TP/TV_USB)
OC6#	USB12~13(N/A)
OC7#	GPIO14

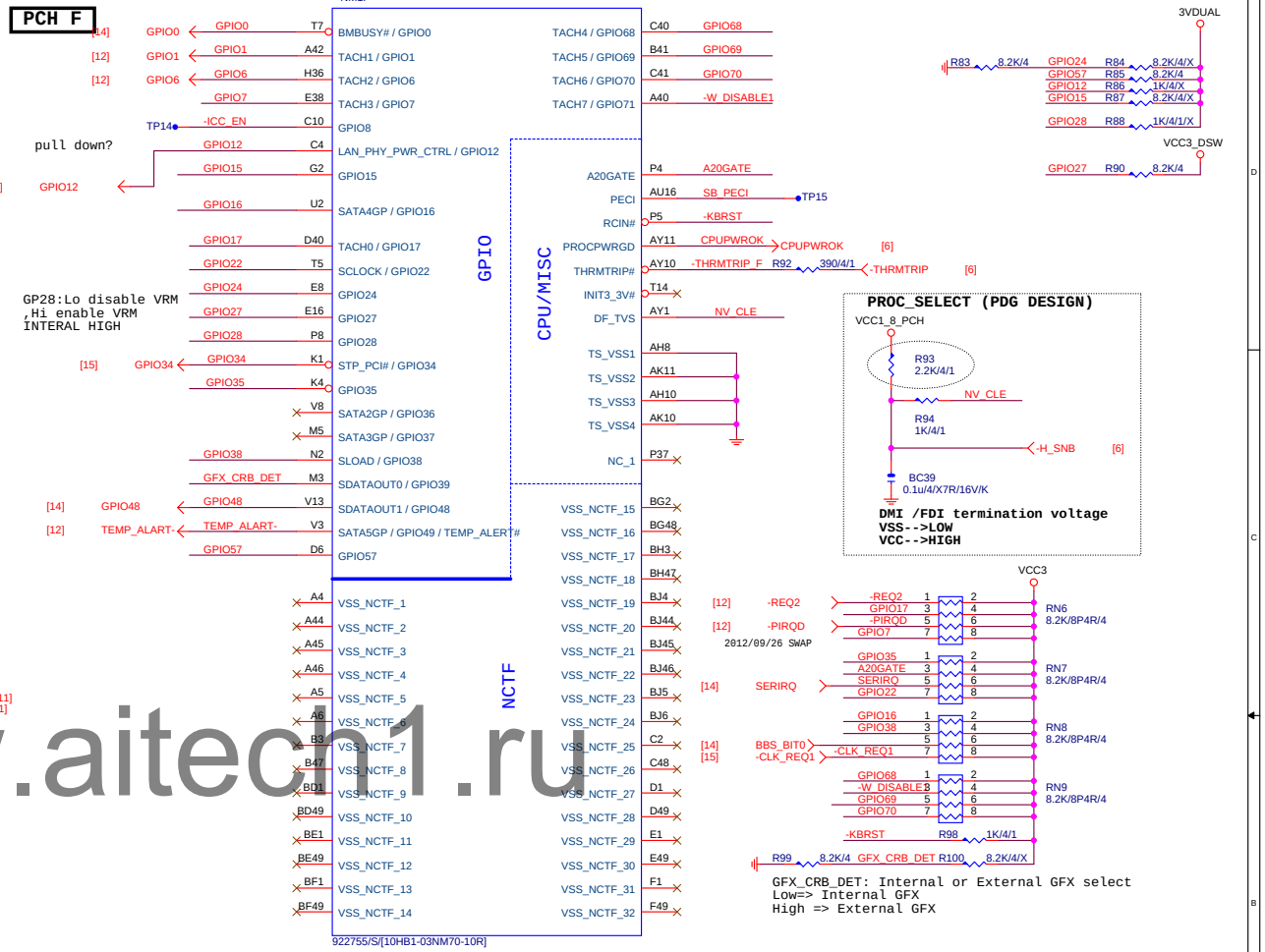
GIGABYTE TECHNOLOGIES , INC.

Title	PCH FDI,DMI,USB ,PCIE,NVRAM	
Size: Custom	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 12 of 25	

PCH D DISPLAY



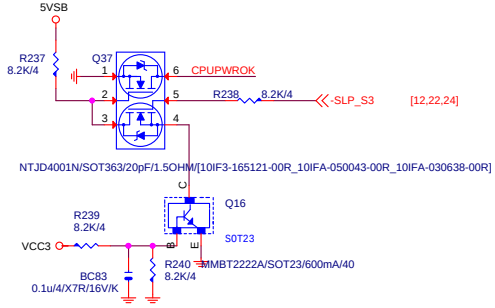
PCH F



VGA ESD

VGA SIGNAL

CPUPWROK



GIGABYTE TECHNOLOGIES , INC.		
Title: PCH DISPLAY ,CLK BUFFER		
Size: Custom	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 13 of 25	

PCH A

HM70/NM70 SATA3.0 ONLY PORT0
FOR 4PORT SKU PORT 1,3 DISABLE

BBS_BIT0: BIOS Boot Strap Bit 0

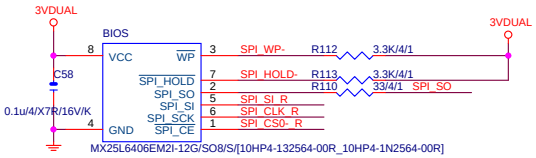
PCH HS

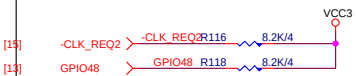
Boot BIOS Strap

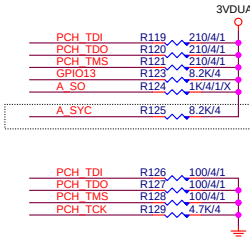
PCI_GNT#1	BBS_BIT0	Boot BIOS Location
1	1	SPI (Default)
0	1	Reserved (NAND)
0	0	LPC

1 means floating
0 means PD 1K

BIOS



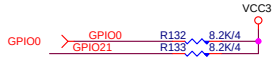




HDA_SDOUT: Flash Descriptor Security Overide
Low (Default) ==> Disabled
High ==> Enabled

A_SYC: PLL ODVR Voltage
Low (Default) ==> 1.8V
High ==> 1.5V

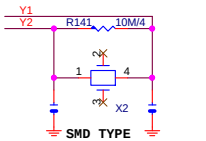
ICH_INTVRMEN: Integrated SUS 1.05V VRM Enable
High ==> Enabled internal VRs
Low ==> Enabled external VRs



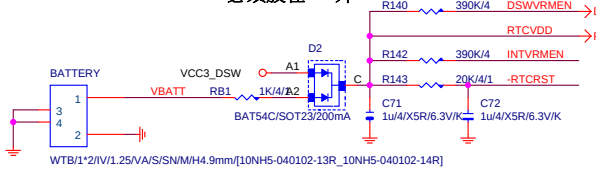
BATTERY

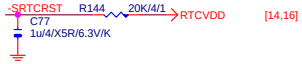
CR2032/[11BL5-032032-31R_11BL5-032032-32R]

RB 必須放在BAT外



32.768K/12.5p/20ppm/8*3.8/50K/S
C69 18p/4/NPO/50V/J
C70 18p/4/NPO/50V/J





Company	GIGABYTE TECHNOLOGIES , INC.
Title	PCH HOST , SATA, PCI
Size	Custom
Document Number	MRNM7AP
Rev	1.0
Date	Thursday, May 02, 2013
Sheet	14 of 25

PCH B

NM1B

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

LAN

LAN_GPPRXN [19]
LAN_GPPRXP [19]
LAN_GPPTXN [19]
LAN_GPPTXP [19]

0.1u/4/X7R/16V/K C78 PET_N1
0.1u/4/X7R/16V/K C79 PET_P1

PCIEMIN1_RXN [20]
PCIEMIN1_RXP [20]
PCIEMIN1_TXN [20]
PCIEMIN1_TXP [20]

0.1u/4/X7R/16V/K C82 PET_N3
0.1u/4/X7R/16V/K C83 PET_P3

PERN1 BG34
PERP1 BJ34
PETN1 AV32
PETP1 AU32
PERN2 BE34
PERP2 BF34
PETN2 BB32
PETP2 AY32
PERN3 BG36
PERP3 BJ36
PETN3 AV34
PETP3 AU34
PERN4 BF36
PERP4 BE36
PETN4 AY34
PETP4 BB34
PERN5 BG37
PERP5 BH37
PETN5 AY36
PETP5 BB36
PERN6 BJ38
PERP6 BG38
PETN6 AU36
PETP6 AV36
PERN7 BG40
PERP7 BJ40
PETN7 AY40
PETP7 BB40
PERN8 BE38
PERP8 BC38
PETN8 AW38
PETP8 AY38

HM/NM70 5~8 PORT DISABLE

SMBALERT# / GPIO11 E12 GPIO11
SMBCLK H14 SMBCLK → SMBCLK [8,20]
SMBDATA C9 SMBDATA → SMBDATA [8,20]

SML0ALERT# / GPIO60 A12 DRST_S3_CTRL
SML0CLK C8 SML0CLK
SML0DATA G12 SML0DAT → SML0DAT [12]

SML1ALERT# / PCHHOT# / GPIO74 C13 -PCH_HOT
SML1CLK / GPIO58 E14 SML1CLK → SML1CLK [12]
SML1DATA / GPIO75 M16 SML1DAT

CL_CLK1 M7
CL_DATA1 T11
CL_RST1# P10

3VDUAL

SMBCLK R146 1K/4/1
SMBDATA R147 1K/4/1
DRST_S3_CTRL R148 8.2K/4
-CLK_REQ5 1 2
-CLK_REQ4 3 4
-PCH_HOT 5 6
GPIO11 7 8
RN10 8.2K/8P4R/4

LAN

PCIE_LAN_CLKN [19] → CLKOUT_PCIE0N Y40
PCIE_LAN_CLKP [19] → CLKOUT_PCIE0P Y39

-CLK_REQ0 → PCIECLKRQ0# / GPIO73 J2

CLKOUT_PCIE1N AB49
CLKOUT_PCIE1P AB47

[13] -CLK_REQ1 → -CLK_REQ1 → PCIECLKRQ1# / GPIO18 M1

Mini_PCIE

mPCIE1_CLK [20] → CLKOUT_PCIE2N AA48
-mPCIE1_CLK [20] → CLKOUT_PCIE2P AA47

[14] -CLK_REQ2 → -CLK_REQ2 → PCIECLKRQ2# / GPIO20 V10

CLKOUT_PCIE3N Y37
CLKOUT_PCIE3P Y36

-CLK_REQ3 → PCIECLKRQ3# / GPIO25 A8

CLKOUT_PCIE4N Y43
CLKOUT_PCIE4P Y45

-CLK_REQ4 → PCIECLKRQ4# / GPIO26 L12

CLKOUT_PCIE5N V45
CLKOUT_PCIE5P V46

-CLK_REQ5 → PCIECLKRQ5# / GPIO44 L14

CLKOUT_PEG_B_N AB42
CLKOUT_PEG_B_P AB40

-CLK_REQB → PEG_B_CLKRQ# / GPIO56 E6

CLKOUT_PCIE6N V40
CLKOUT_PCIE6P V42

PCH_GPIO45 → PCIECLKRQ6# / GPIO45 T13

CLKOUT_PCIE7N V38
CLKOUT_PCIE7P V37

-CLK_REQ7 → PCIECLKRQ7# / GPIO46 K12

CLKOUT_ITPXDP_N AK14
CLKOUT_ITPXDP_P AK13

PEG_A_CLKRQ# / GPIO47 M10 CLK_PEGA_OE-

CLKOUT_PEG_A_N AB37
CLKOUT_PEG_A_P AB38

[13] GPIO34 → GPIO34 R151 8.2K/4

VCC3
3VDUAL

PCH_GPIO45 1 2 RN11 8.2K/8P4R/4
SML1DAT 3 4
-CLK_REQ0 5 6
7 8

CLK_REQB 1 2 RN12 8.2K/8P4R/4
SML0CLK 3 4
-CLK_REQ3 5 6
-CLK_REQ7 7 8

CLK_PEGA_OE- R154 8.2K/4

CLKOUT_DMI_N AV22 -CLK_CPU → -CPUCLK [6]
CLKOUT_DMI_P AU22 CLK_CPU → CPUCLK [6]

CLKOUT_DP_N AM12 -DPLL_CPU → -DPLLCLK [6]
CLKOUT_DP_P AM13 DPLL_CPU → DPLLCLK [6]

CLKIN_DMI_N BF18 -SRCCLK_PCH R152 8.2K/4
CLKIN_DMI_P BE18 SRCCLK_PCH R153 8.2K/4

CLKIN_GND1_N BJ30 -CLK_GND R155 8.2K/4
CLKIN_GND1_P BG30 CLK_GND R157 8.2K/4

CLKIN_DOT_96N G24 -DOTCLK R158 8.2K/4
CLKIN_DOT_96P E24 DOTCLK R159 8.2K/4

CLKIN_SATA_N AK7 -SRCCLK_SATA R160 8.2K/4
CLKIN_SATA_P AK5 SRCCLK_SATA R161 8.2K/4

REFCLK14IN K45 PCHCLK14 R162 8.2K/4

CLKIN_PCILOOPBACK H45 PCH33 → PCH33 [12]

XTAL25_IN V47 XTALI_PCH
XTAL25_OUT V49 XTALO_PCH

XTALI_PCH
R163 1M/4
3 2 1XTALO_PCH
4
LX2 SMD TYPE
25M/20p/30ppm/3.2*2.5/70/S/[10XT5-825000-50R_10XT6-125000-10R_10XT5-D25000-00H]
C86 27p/4/NPO/50V/J
C87 27p/4/NPO/50V/J

XCLK_RCOMP Y47 CLK_RCOMP R164 90.9/4/1 → VCC1_05_PCH

CLKOUTFLEX0 / GPIO64 K43
CLKOUTFLEX1 / GPIO65 F47
CLKOUTFLEX2 / GPIO66 H47
CLKOUTFLEX3 / GPIO67 K49 PCH_48M R166 33/4 → LPCCLK48 [18]

native 48Mhz

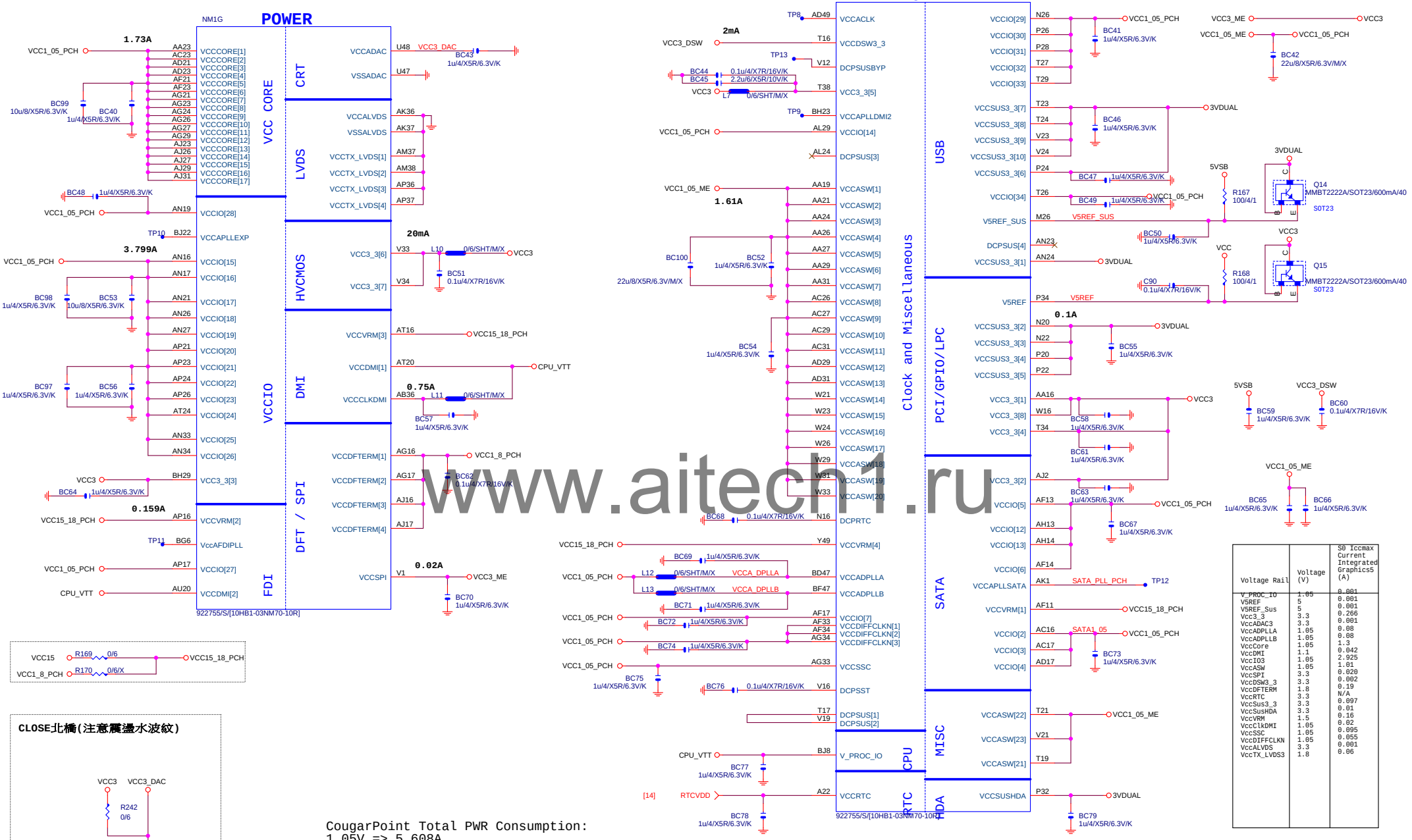
all the CLKRQ# signals are Mobile Only.

922755/S/[10HB1-03NM70-10R]

Flex0,2 : 33MHZ
Flex1,3 :
27/14/24/48/25MHZ

GIGABYTE TECHNOLOGIES , INC.		
Title: PCH GPIO , CTRL , AUDIO		
Size: Custom	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 15 of 25	

PCH G,J POWER



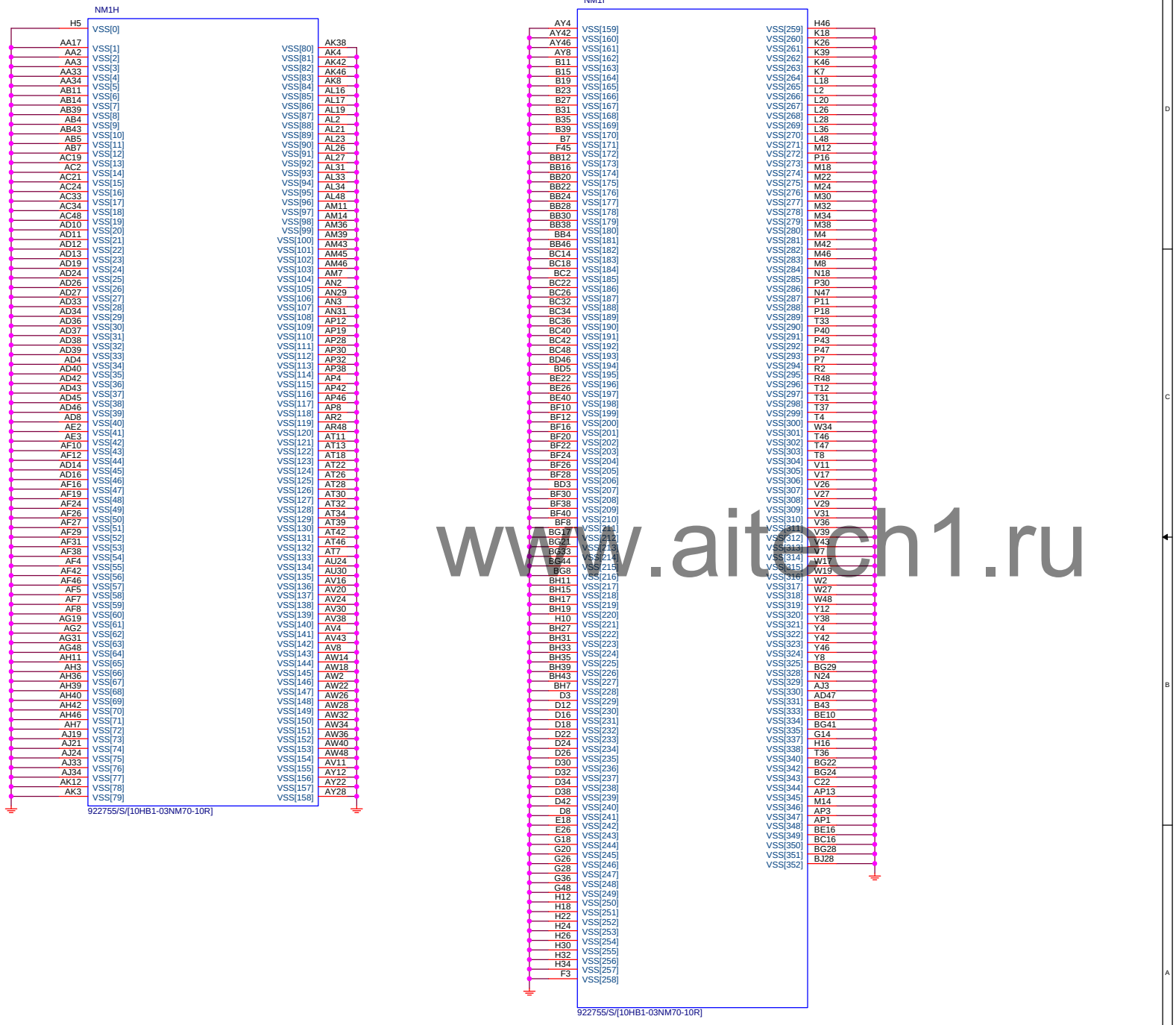
Voltage Rail	Voltage (V)	S0 Iccmax Current Integrated Graphics5 (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	N/A
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

CougarPoint Total PWR Consumption:
1.05V => 5.608A
5V => 0.002A
3.3V => 0.399A
1.8V => 0.25A
1.5V => 0.16A

CLOSE北橋(注意覆蓋水波紋)

GIGABYTE TECHNOLOGIES , INC.			
Title: PCH PWR ,GND			
Size: Custom	Document Number: MRNM7AP		Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 16 of 25		

PCH H,I GND



GIGABYTE TECHNOLOGIES , INC.		
Title: PCH ,GND		
Size: Custom	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 17 of 25	

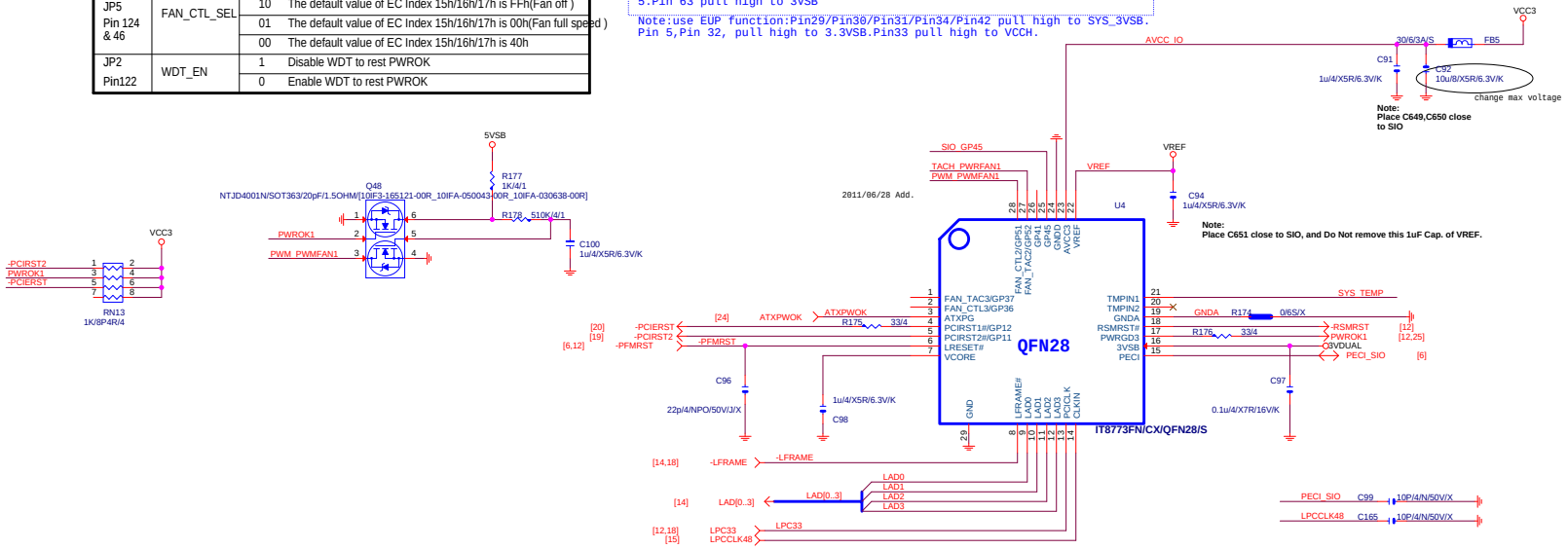
Power On Strapping Options

Symbol		value	Description
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 80h
		10	The default value of EC Index 15h/16h/17h is FFh(Fan off)
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 40h
JP2 Pin122	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK

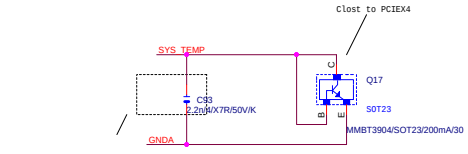
If without use these pins, Please pull-up. Don't let it floating
1.Pin 6:ATXPG
2.Pin 29:SUSB#
3.Pin 21/ Pin 57/ Pin 59/ Pin61
4.Pin37-40 KCLK/KDAT/MCLK/MDAT

5.Pin 63 pull high to 3VSB

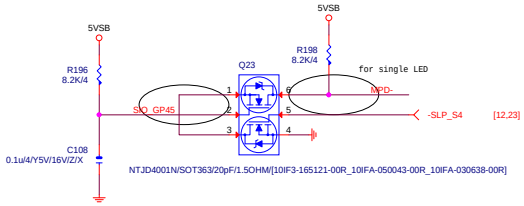
Note:use EUP function:Pin29/Pin30/Pin31/Pin34/Pin42 pull high to SYS_3VSB.
Pin 5,Pin 32, pull high to 3.3VSB.Pin33 pull high to VCCH.

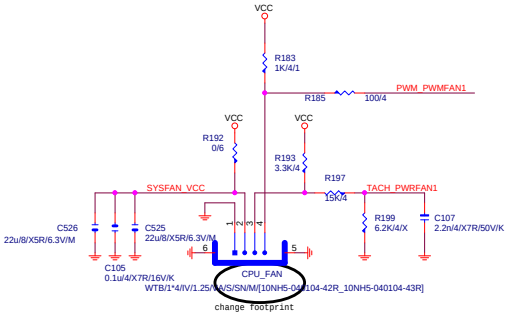


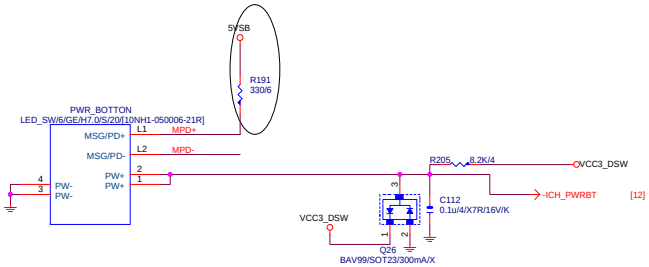
TEMP H/W MONITOR



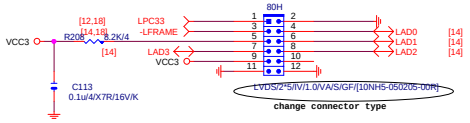
Please close to SIO



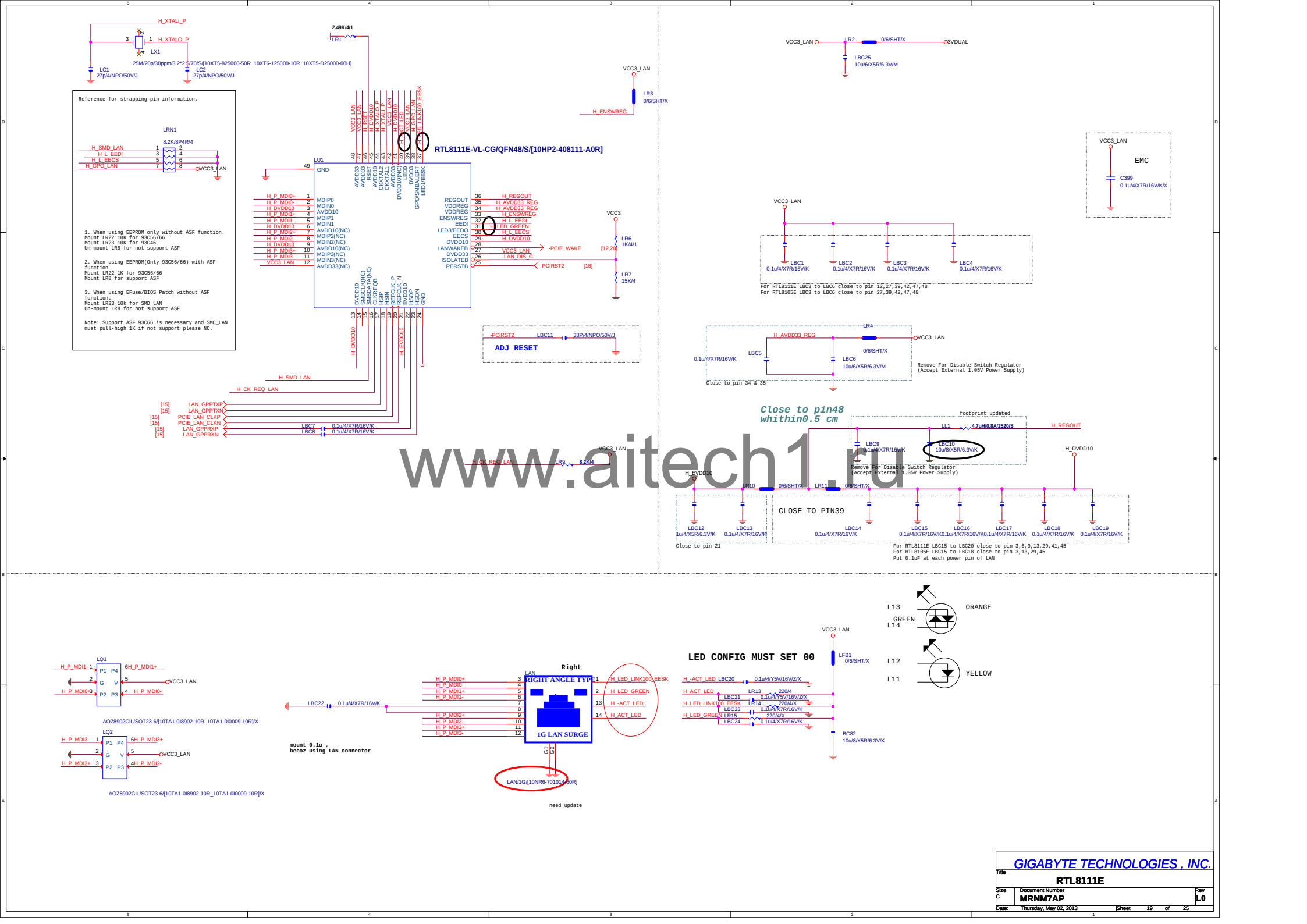




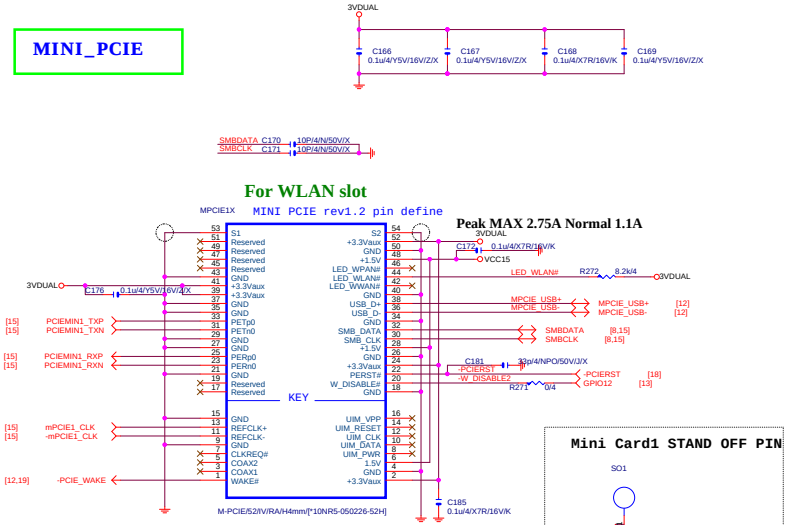
80H



GIGABYTE TECHNOLOGIES , INC.			
Title: ITE8773,FAN,FP			
Size: Custom	Document Number: MRNM7AP		Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 18 of 25		

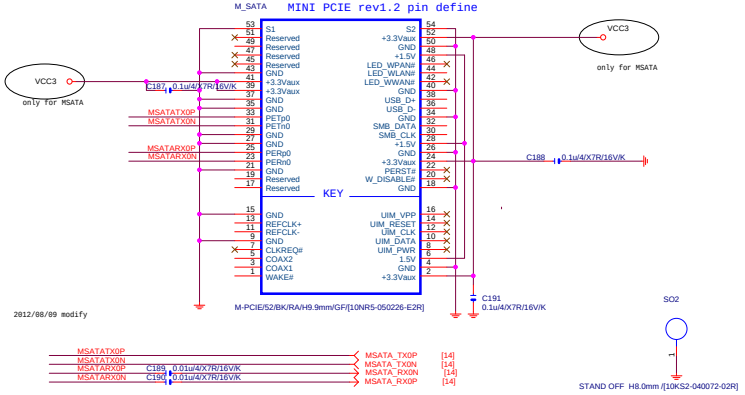


MINI_PCIE

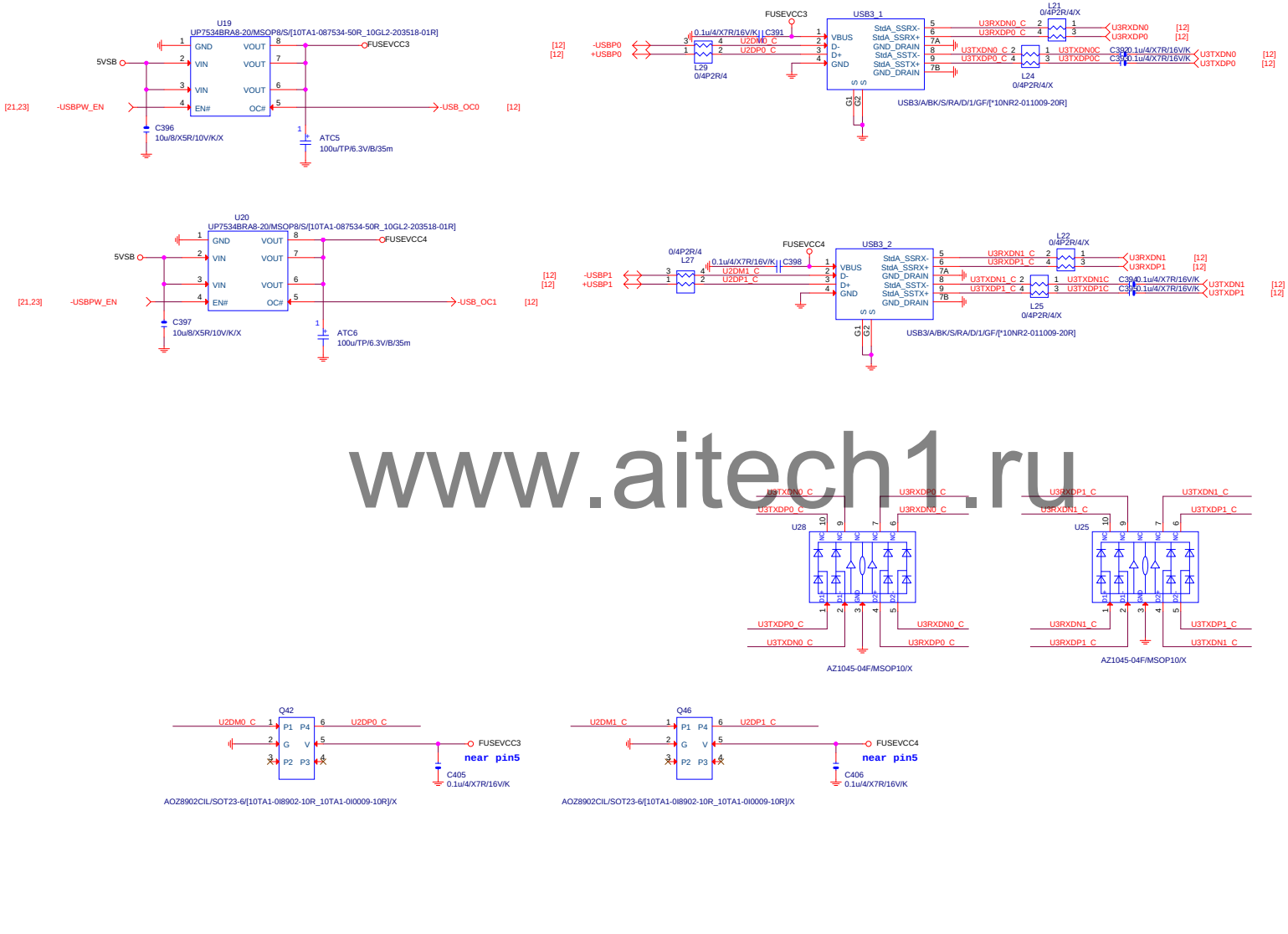


MSATA

EXT_CON PWR CIRCUIT



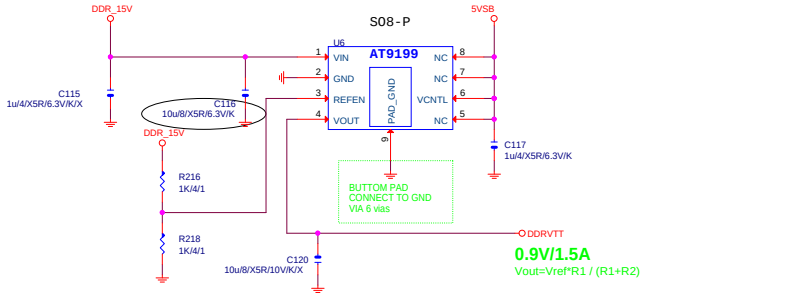
GIGABYTE TECHNOLOGIES , INC.		
Title: MINI-PCIE & PCIE& EXT_CON		
Size: Custom	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 20 of 25	



GIGABYTE TECHNOLOGIES , INC.		
Title: FRONT & REAR USB		
Size: Custom	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 21 of 25	

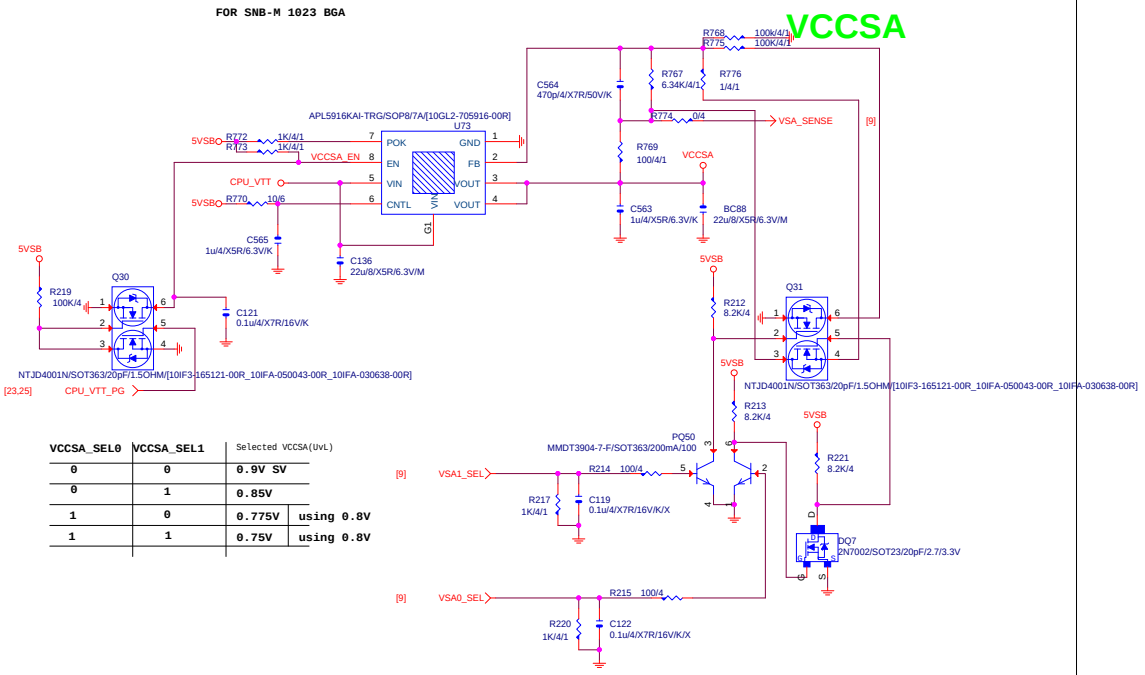
DDRVTT

DDR3 0.75V/0.83A



FOR SNB-M 1023 BGA

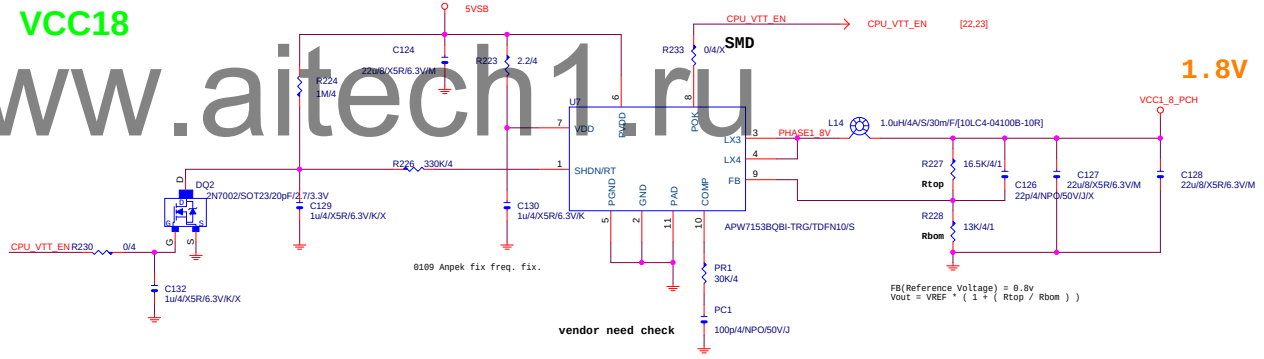
VCCSA



VCCSA_SEL0	VCCSA_SEL1	Selected VCCSA(UvL)	
0	0	0.9V SV	
0	1	0.85V	
1	0	0.775V	using 0.8V
1	1	0.75V	using 0.8V

5VDUAL

VCC18



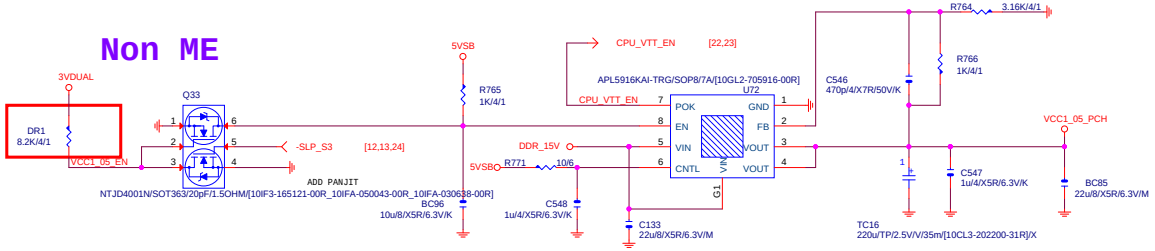
1.8V

VCC1_05

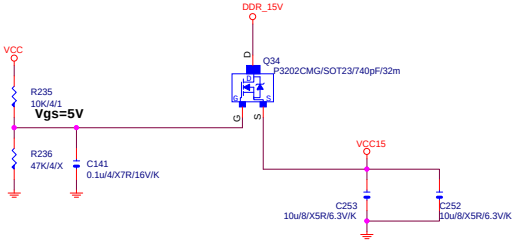
Note.

Non AMT model:
R225 remove.
DQ2.R230.C132.DR1 use.

Non ME

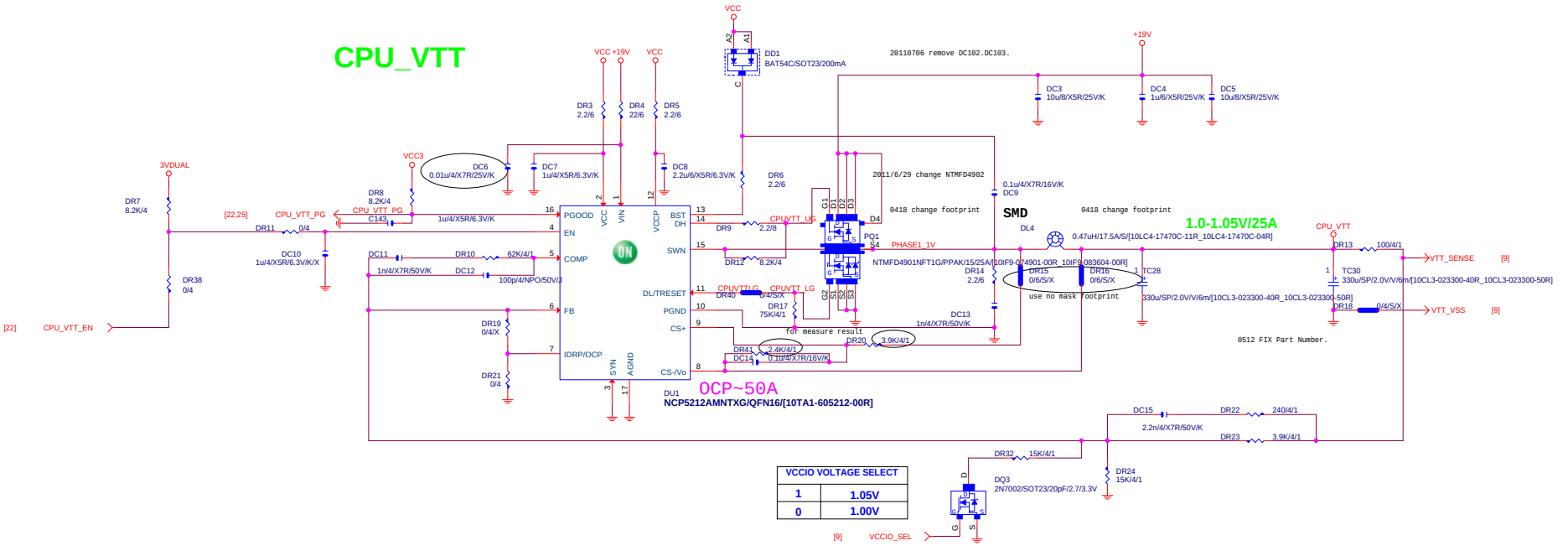


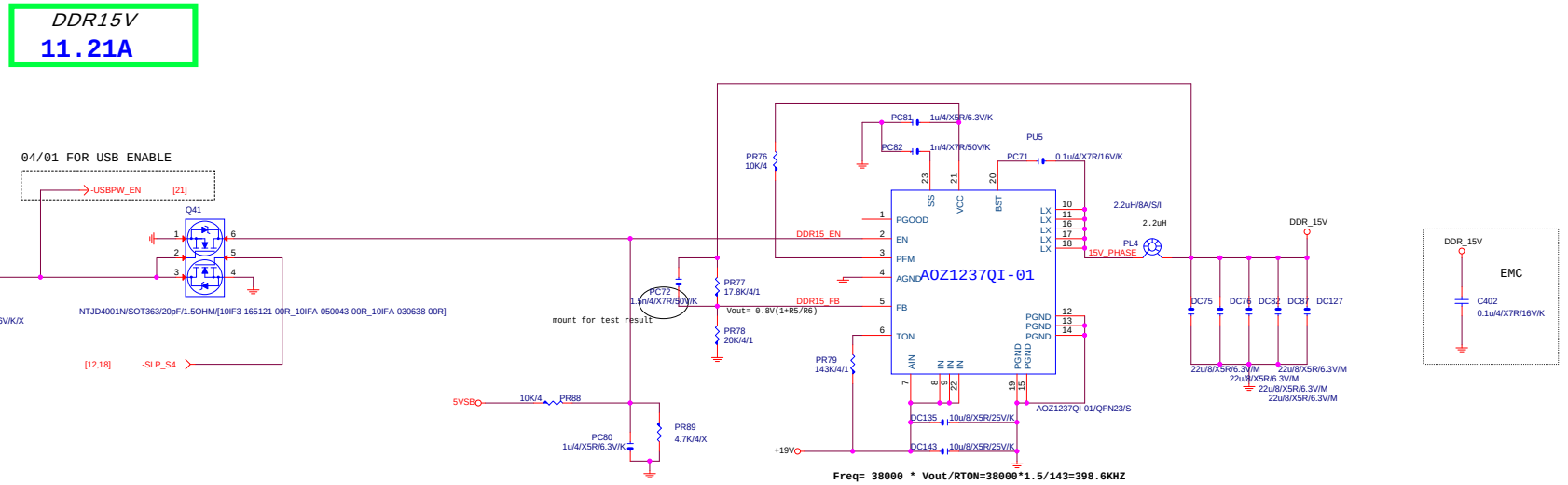
VCC15&VCC12



Title	LINNER-POWER-1		
Size	Document Number MRNM7AP		Rev 1.0
Date: Thursday, May 02, 2013		Sheet 22 of 25	

GIGABYTE TECHNOLOGIES , INC.





GIGABYTE TECHNOLOGIES , INC.	
Title	DISCRETE POWER
Size C	Document Number MRNM7AP Rev 1.0
Date: Thursday, May 02, 2013	Sheet 23 of 25

AD19V

FOR INOUT AD PROTECT CIRCUIT

P-MOSFET

P2003EEA/QFN3*3/1590pF/20m/[10IF9-202003-00R_10IF9-123305-00R]

For 120W solution
10A

TVM2B270K33LRY/0805/22V/330P/S/[10RS3-223300-00R]

PU2 設定 H =22 V L= 10.1V

APM2315AC-TRL/SOT23/1135pF/55m

change low to 10.1V

GS7138S8-5P0-R/SOT89/150mA/[10LG8-017138-00R]

DC-PW/2P/BK/RA/D/Snf/[11NR4-030002-70R]

LDO VIN MAX SPEC MUST >25V

8720 EMI Fix.

8710 Swap.

HOLE

K1_ICT/X

HOLE_3/X

add new footprint

COUPON1 Single END 4 mils 50 ohm +- 15% TOP

COUPON2 Single END 4 mils 50 ohm +- 10% INT

COUPON3 Single END 4 mils 50 ohm +- 10% INT2

COUPON4 Single END 4 mils 50 ohm +- 10% INT3

COUPON5 Single END 4 mils 50 ohm +- 10% INT4

COUPON6 Single END 4 mils 50 ohm +- 15% BOT

VCC&VCC3

SM3317NSQGC/QFN3*3/910pF/11.5m/[10IF9-113317-00R_10IF9-090903-00R]

NMOSFET

2N7002/SOT23/20pF/2.7/3.3V

for T229 fail

correct "+/-"

ATX PPOWER GOOD

for ATXPWOK rising

NTJD4001N/SOT363/20pF/1.5OHM/[10IF3-165121-00R_10IFA-050043-00R_10IFA-030638-00R]

0717 Fix for DQA measure.

5VSB

Voltage level : 5V
Max current : 13A

AOZ1237QI-01

change max voltage

mount for test result

On threshold 2.5V

Freq= 38000 * Vout/RTON=38000*5/475=400KHZ

3VDUAL

Voltage level : 3.3V
Max current : 13A

Freq= 38000 * Vout/RTON=38000*3.3/475=396.84KHZ

APL5315BI-TRL/SOT23-5/300mA

ADD PANJIT

EMC

GIGABYTE TECHNOLOGIES , INC.	
Title	AD19V & VCC & VCC3
Size: Custom	Document Number: MRNM7AP
Rev	1.0
Date: Thursday, May 02, 2013	Sheet 24 of 25

Vcore loadline=5.9 m ohm
Vaxg loadline=4.1 m ohm

NCP6131 VR12 POWER CKT - 1+1 PHASE

PWM ADDRESS		
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL	SVID ADDRESS FOR V_GT RAIL
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
125K	1010	1011
165K	1100	1101

BOOT VOLTAGE	
RESISTOR VALUE	BOOT VOLTAGE
10K	0V
25K	0.9V
45K	1V
70K	1.1V
95K	1.2V
125K	1.35V
165K	1.5V
VCC	SHUTDOWN

VCORE VBOOT SET AT 0 V

V_GT IMAX SET AT 18A

PWM ADDRESS

VCORE IMAX SET AT 33A

OC

VCORE PORTION

V_GT PORTION

Refer Intel design guide

BOTTOM PAD CONNECT TO GND Through 4 VIAs

PUT COLSE TO V_GT HOT SPOT

please close MOS

PUT COLSE TO VCORE HOT SPOT

please close MOS

Work F= 380Khz

Placement close to U2

17W CPU power spec :
Vcore: Iccmax = 33A ;TDC = 21.5A
Loadline = 2.9m ohm
Vboot = 0 A OCP = 50A

VGFX : Iccmax = 18A ;TDC = 12A
Loadline = 4.6m ohm
Vboot = 0 A; OCP = 29A

Please close to CPU

GIGABYTE TECHNOLOGIES , INC.

Title	VCORE&VGFX NCP6131	
Size: Custom	Document Number: MRNM7AP	Rev: 1.0
Date: Thursday, May 02, 2013	Sheet 25 of 25	